WHAT IS CLAIMED IS:

1. A duplexing method in a system duplexed into a first unit and a second unit, the first unit including a first processor and a first local memory, and the second unit including a second processor and a second local memory, the method comprising the steps of:

providing a duplexing channel for concurrently accessing and selectively accessing the first local memory and the second local memory between the first unit and the second unit;

providing a duplexing control logic section accessible to the first local memory and the second local memory through the duplexing channel; and

concurrently accessing the first local memory and the second local memory through the duplexing channel by the duplexing control logic section based on a request for memory accessing by an active processor, which is one of the first processor and the second processor.

2. The duplexing method of claim 1, wherein the duplexing channel comprises:

a data channel for transmitting data, an address thereof, and a related control signal while concurrently writing in the first local memory and the second local memory; and

a control channel for active/standby negotiation and exchange of information between the duplexed first and second units, and for transmitting and receiving signals informing of a status of the first and the second units, a status of duplexed connection, and signals informing start and termination of a duplexing cycle for control in a hardware like manner after the negotiation of duplexing.

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3.   A duplexing method in a system duplexed into a first unit and a second unit, the first unit and the second unit including a first local memory and a second local memory, respectively, the method comprising the steps of:

5   mutually requesting responses on a status of each other between a first processor and a second processor included in the first unit and the second unit, respectively;

operating as an active processor if no response is received from the other processor;

operating as a standby processor if a response is received from the other processor;

10   transmitting a confirming signal by the standby processor to inform the active processor of a normal operation of the standby processor; and

concurrently and selectively accessing the first local memory and the second local memory by the active processor in accordance with reception of the confirming signal if there is a request for memory access.

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4.   The duplexing method of claim 3, characterized by concurrently accessing the first local memory and the second local memory if there is a request for memory access after the active processor receives the confirming signal informing that the standby processor is in a normal operation state.

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5.   A duplexing method in a large scale system including duplexed first and second units with identical construction, the first unit including a first processor and a first local memory, and the second unit including a second processor and a second local memory, comprising:

25   a duplexing channel for concurrently and selectively accessing the first local

memory and the second local memory between the first and the second units; and

a duplexing control logic section for concurrently and selectively accessing the first local memory and the second local memory through the duplexing channel based on a request for memory access by an active processor, which is either the first processor or the second processor.

6. The duplexing method of claim 5, wherein the duplexing channel comprises:

a data channel for transmitting data, which is transmitted by the duplexing control logic section when concurrently writing in the first local memory and the second local memory, an address thereof and a related control signal; and

a control channel used by the first processor and the second processor for active/standby negotiation and exchange of information between the duplexed first and second units, and for transmitting and receiving signals informing status of the first and the second units, signals informing status of duplexed connection, and signals informing start and termination of a duplexing cycle for control in a hardware like manner after negotiation of duplexing.

7. The duplexing method of claim 5, further comprising:

local buffers respectively included in the duplexed first and second units for buffering a control signal, an address and data used for accessing the local memory thereof; and

local buffers respectively included in the duplexed first and second units for buffering a control signal, an address and data for accessing the duplexed other local memory.